CLAIMS

What is claimed is:

1. A semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each of the plurality of signal connection devices is positioned in one of the plurality of cavities and the active surfaces of the plurality of semiconductor dice are adhered to the top surface of the substrate, and wherein a plurality of openings is formed in the bottom surface of the substrate exposing the plurality of signal connection devices therethrough; and

a molding layer over the top surface of the substrate and the back surfaces of the plurality of semiconductor dice.

2. The semiconductor device package of claim 1, further comprising:

a first dielectric layer upon the bottom surface of the substrate; and

a plurality of openings in the first dielectric layer exposing the plurality of signal connection devices therethrough.

3. The semiconductor device package of claim 2, wherein the substrate includes a silicon wafer.

4. The semiconductor device package of claim 3, wherein the plurality of signal connection devices is selected from the group consisting of gold stud bumps, copper stud bumps, and plated stud bumps.

5. The semiconductor device package of claim 4, wherein each of the plurality of cavities exhibits a depth which is at least as great as or greater than a height of each of the plurality of signal connection devices.

6. The semiconductor device package of claim 5, further comprising a layer of die attach material disposed between the active surface of each of the plurality of semiconductor dice and the top surface of the substrate.

7. The semiconductor device package of claim 6, wherein the layer of die attach material comprises an epoxy material.

8. The semiconductor device package of claim 6, wherein the layer of die attach material comprises a polyimide material.

9. The semiconductor device package of claim 6, wherein the layer of die attach material comprises benzocyclobutene.

10. The semiconductor device package of claim 6, wherein the layer of die attach material exhibits a dielectric constant of up to about three.

11. The semiconductor device package of claim 10, wherein the molding layer comprises a material which is capable of withstanding a temperature of up to about 300° C without substantial degradation thereof.

12. The semiconductor device package of claim 2, further comprising:

a first circuit layer over the first dielectric layer electrically connected to the plurality of signal connection devices;

at least one additional dielectric layer, having at least one additional plurality of openings formed therethrough; and

at least one additional circuit layer over the at least one additional dielectric layer electrically coupled with the first circuit layer;

an outermost dielectric layer having a plurality of holes formed therethrough, the outermost dielectric layer being disposed over the at least one additional circuit layer; and

a plurality of conductive bumps disposed in the plurality of holes of the outermost dielectric layer and electrically coupled with the at least one additional circuit layer.

13. A memory device comprising:

a carrier substrate;

a plurality of electrical contacts coupled with electrical circuitry formed in the carrier substrate; and

at least one semiconductor device package coupled with the electrical circuitry in the carrier substrate, the at least one semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each of the plurality of signal connection devices is positioned in one of the plurality of cavities and the active surfaces of the plurality of semiconductor dice are adhered to the top surface of the substrate, and wherein a plurality of openings is formed in the bottom surface of the substrate exposing the plurality of signal connection devices therethrough; and

a molding layer over the top surface of the substrate and the back surfaces of the plurality of semiconductor dice.

14. A computing system comprising:

a carrier substrate;

a processor operably coupled to the carrier substrate;

at least one input device operably coupled with the carrier substrate;

at least one output device operably coupled with the carrier substrate; and

a memory device operably coupled to the carrier substrate, the memory device including at least one semiconductor device package, the at least one semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each of the plurality of signal connection devices is positioned in one of the plurality of cavities and the active surfaces of the plurality of semiconductor dice are adhered to the top surface of the substrate, and wherein a plurality of openings is formed in the bottom surface of the substrate exposing the plurality of signal connection devices therethrough ; and

a molding layer over the top surface of the substrate and the back surfaces of the plurality of semiconductor dice.

15. A semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die of the plurality having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each semiconductor die of the plurality is disposed in one of the plurality of cavities such that the back surface of each semiconductor die is facing the base of its respective one of the plurality of cavities;

a first dielectric layer disposed upon the top surface of the substrate and upon the active surface of each of the plurality of semiconductor dice; and

a plurality of openings in the first dielectric layer exposing the plurality of signal connection devices.

16. The semiconductor device package of claim 15, wherein the substrate comprises a silicon wafer.

17. The semiconductor device package of claim 16, wherein the plurality of signal connection devices comprises bond pads.

18. The semiconductor device package of claim 17, wherein each of the plurality of cavities exhibits a same depth which is at least equal to or greater than a height of each the plurality of semiconductor dice.

19. The semiconductor device package of claim 18, further comprising a layer of die attach material disposed between and adhering the active surface of each of the plurality of semiconductor dice and the top surface of the substrate.

20. The semiconductor device package of claim 19, wherein the layer of die attach material comprises an epoxy material.

21. The semiconductor device package of claim 19, wherein the layer of die attach material comprises a polyimide material.

22. The semiconductor device package of claim 19, wherein the layer of die attach material comprises benzocyclobutene.

23. The semiconductor device package of claim 19, wherein the layer of die attach material further comprises a material exhibiting a dielectric constant of up to about three.

24. The semiconductor device package of claim 15, further comprising:

a first circuit layer over the first dielectric layer electrically connected to the plurality of signal connection devices;

at least one additional dielectric layer, having at least one additional plurality of openings formed therethrough; and

at least one additional circuit layer over the at least one additional dielectric layer electrically coupled with the first circuit layer;

an outermost dielectric layer having a plurality of holes formed therethrough, the outermost dielectric layer being disposed over the at least one additional circuit layer; and

a plurality of conductive bumps disposed in the plurality of holes of the outermost dielectric layer and electrically coupled with the at least one additional circuit layer.

25. A memory device comprising:

a printed circuit board;

a plurality of electrical contacts coupled with electrical circuitry formed in the printed circuit board; and

at least one semiconductor device package coupled with the electrical circuitry in the printed circuit board, the at least one semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die of the plurality having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each semiconductor die of the plurality is disposed in one of the plurality of cavities such that the back surface of each semiconductor die is adhered to the base of its respective one of the plurality of cavities;

a first dielectric layer disposed upon the top surface of the substrate and upon the active surface of each of the plurality of semiconductor dice; and

a plurality of openings in the first dielectric layer exposing the plurality of signal connection devices.

26. A computing system comprising:

a printed circuit board;

a processor operably coupled to the printed circuit board;

at least one input device operably coupled with the printed circuit board;

at least one output device operably coupled with the printed circuit board; and

a memory device operably coupled to the printed circuit board, the memory device including at least one semiconductor device package, the at least one semiconductor device package comprising:

a plurality of semiconductor dice, each semiconductor die of the plurality having a back surface, an active surface and a plurality of signal connection devices on the active surface;

a substrate having a top surface, a bottom surface and a plurality of cavities formed in the top surface of the substrate, wherein each semiconductor die of the plurality is disposed in one of the plurality of cavities such that the back surface of each semiconductor die is adhered to the base of its respective one of the plurality of cavities;

a first dielectric layer disposed upon the top surface of the substrate and upon the active surface of each of the plurality of semiconductor dice; and

a plurality of openings in the first dielectric layer exposing the plurality of signal connection devices.